ENGLISH TRANSLATION OF CLAIMS & DETAILED DESCRIPTION OF: JP 11-514163 A; Corresponds with US 5,990,709 A

CLAIMS

[Claim(s)]
1. It is Circuit Apparatus for Measuring Two Quantity of Electricity Which Can Realize the 1st Neurone Metal Oxide Silicon Field Effect Transistor (M1) and Criteria Transistor (R). One current mirror (SP) is prepared. The output side (AM1) of said 1st neurone metal oxide silicon field effect transistor (M1) minds the 1st connection terminal (1). Connect with the output side (ASP) of said current mirror (SP), and the output side (AR) of said criteria transistor (R) is connected to the input side (ESP) of said current mirror (SP). Said 1st connection terminal (1) is connected to at least one control connection terminal (ST) of an inverter stage (IS), and a signal (ES) appears in the output side (AIS) of this inverter stage as a result of a comparison. Circuit apparatus characterized by things.
2. The 1st switch unit (S1) connected to said 1st connection terminal (1) and the control connection terminal (ST) of said inverter stage (IS) is prepared. Circuit apparatus according to claim 1.
3. The 2nd switch unit (S2) is prepared and the 1st connection terminal (A1S2) of this 2nd switch unit (S2) is connected to the input side (EM1) of said 1st neurone metal oxide silicon field effect transistor (M1), and the input side (ER) of said criteria transistor (R) through the 2nd connection terminal (2) in this case. Circuit apparatus according to claim 1 or 2.
4. Said criteria transistor (R) is formed of the 2nd neurone metal oxide silicon field effect transistor (M2). Circuit apparatus given [to claims 1-3] in any 1 term.
5. Said criteria transistor (R) is formed of a metal oxide silicon field effect transistor (M2). Circuit apparatus given [to claims 1-3] in any 1 term.
6. Said the 1st switch unit (S1) and/or said 2nd switch unit (S2) consist of a metal oxide silicon field effect transistor. Circuit apparatus given [to claims 2-5] in any 1 term.
7. Said the 1st switch unit (S1) and said 2nd switch unit (S2) are controlled by the common control signal (phi). Circuit apparatus given [to claims 1-4] in any 1 term.
8. The buffer unit for storing a signal (ES) temporarily said result is prepared, and the input side of this buffer unit is connected to the output side (AIS) of said inverter stage (IS). Any 1 term or the circuit apparatus according to claim 6 or 7 to claims 1-4.
9. The buffer unit for storing a signal (ES) temporarily said result is prepared, and the input side of this buffer unit is connected to the output side (AIS) of said inverter stage (IS). Any 1 term or the circuit apparatus according to claim 5, 6, or 7 to claims 1-3.
10. Multiplication Child Bit (Va1) as Input Potential, Multiplicand Bit (Va2), Sum Bit (Vb) of Partial Product to Precede, and Transfer Bit of Partial Product to Precede (Vc)
) を出力和ビット（ｓ）および出力繰越ビット（Ü

In the application of a circuit apparatus given [to claims 1-9 for realizing the binary-multiplication machine cel for carrying out logical combination] in any 1 term,

前記出力繰越ビット（Ü）を形成するための第１

の評価回路（ＢÜ）が設けられており、

the 2nd weighting network (BS) for forming said output sum bit (s) prepares -- having -- **** -- the 2nd inverter stage (IS2) prepares -- having -- **** -- here -- setting -- this -- close [of the 2nd inverter stage (IS2)]
力側に前記出力繰越ビット（Ü）が加えられかつ

this -- the output side of the 2nd inverter stage (IS2) -- negation
れた出力繰越ビット（Ü）が現れ、

Said multiplication child bit (Va1), a multiplicand bit (Va2), the sum bit (Vb) of the partial product to precede, and the transfer bit (Vc) of a partial product to precede are an eclipse with weight.
て前記第１の評価回路（ＢÜ）の前記第１のニュ

ーロンＭＯＳ電界効果トランジスタ（ＭÜ１）の

it adds to a gate connection terminal and the gate connection terminal of said 1st neurone metal oxide silicon field effect transistor (MS1) of said 2nd weighting network (BS) -- having -- and
前記否定された出力繰越ビット（$\bar{Ü}$）は重み付けら

It is added to another gate connection terminal of **** and said 1st neurone metal oxide silicon field effect transistor (MS1) of said 2nd weighting network (BS). Application characterized by things.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
Comparator circuit equipment of two quantity of electricity realizable [with the 1st neurone metal oxide silicon field effect transistor and reference standard] The technical problem that two quantity of electricity is measured mutually is produced in many technical fields. Such a comparison is the foundation of for example, an electrical measurement technique. A threshold type is also technically realizable using a weighting network.
The approach of measuring quantity of electricity using an operational amplifier is well-known, and is often used (U. Tietze, Ch.Schenk, 1990, and page 132-143). Conversion of static loss power has the serious fault of this approach. Another possibility for evaluating two quantity of electricity It is in using a neurone MOS inverter. The basis which should be measured with quantity of electricity of an exception in that case with the change-over threshold of a neurone MOS inverter It is determined (T.). [Shibata, P.Ohmi,] ["A] functional MOS-Transistor featuring gate-level wegheted sum and threshold operations", and IEEE Trans.Electron Devices, 39 and 1992 and page 1444-1455. Using a neurone MOS inverter in this relation has some faults. In the floating gate of the neurone MOS inverter which has VSS+Vth, n<phi F<VDD-Vth, and p, a static shunt current flows to all potential phiF. This usually sometimes corresponds during the actuation period as the threshold gate. Furthermore, threshold selection ****s in a desired property, namely, a technology parameter needs to be controlled very good so that the allowable deviation which needs a threshold electrical potential difference can be maintained.
The technical problem of this invention is measuring quantity of electricity realizable [with a neurone metal oxide silicon field effect transistor] with a basis.
This technical problem is solved by the circuit apparatus according to claim 1.
The circuit apparatus of this invention has the affirmative property of 2 and 3. The level defined also at neither of the times, at the output side of the circuit apparatus of this invention nor the time, does not appear. It is because it is directly switched to a new condition from an old condition. This property is advantageous in continuing data processing in a consecutive stage.
furthermore, in other weighting networks, evaluation comes out so and there is often -- as -- a charge -- minding -- coming out -- there is nothing and it is carried out through a current. The current evaluated is acquired from the potential in the gate (floating) of a transistor. Such potentials can be formed in low resistance in the circuit of ** object. Thereby, the circuit apparatus of this invention can much more ensure evaluation rather than the principle of charge evaluation that it is hard to be influenced to the coupling of a trouble back signal. Thereby, the narrow allowable deviation to the threshold formation at the time of realizing a threshold type can be maintained firmly, for example. because, difference -- it is because it operates in actuation. For example, on it, the very slight potential difference in the 200mV floating gate can be separated certainly, and it can evaluate correctly.

Another advantage of the circuit apparatus of this invention is for a shunt current not to flow in the hibernation of a circuit apparatus. This shows an important advantage compared with many another weighting networks.
When using it for an array circuit, the circuit apparatus of this invention has the advantage of needing only one control-line way, in order to activate the circuit apparatus of this invention.
According to the area comparison with another weighting network, when setting weight to a shunt current degree of freedom at the decoupling list of an output side and an original weighting network, it turns out that the circuit apparatus of this invention is more advantageous. Small or this is clear by the fact as opposed to Boolean part to the circuit apparatus of this invention and that only six transistors and one reference standard which has one another neurone metal oxide silicon field effect transistor or one metal oxide silicon field effect transistor similarly are required.
Another example of this invention is indicated by other claims.
The advantageous example of this invention is shown in the drawing, and is explained below at a detail.
Fig. 1 is a schematic diagram of the circuit apparatus of this invention in that case, Fig. 2 is a schematic diagram in which the use to the multiplier cel of the circuit apparatus of this invention is shown, Fig. 3 is a schematic diagram in which the use in a multiplier cel of the circuit apparatus of this invention is shown, and a transfer bit is directly used for a criteria neurone metal oxide silicon field effect transistor in a multiplier cel in this case.
The circuit apparatus of this invention is explained to a detail based on Figs. 1 thru/or 3.
In Fig. 1, the circuit apparatus of this invention is constituted so that two quantity of electricity realizable [with the 1st neurone metal oxide silicon field effect transistor M1 and reference standard R] may be measured. the :-current mirror SP to which the circuit apparatus of this invention has the following component fundamentally, and - the 1st neurone metal oxide silicon field effect transistor M1, - criteria transistor R, and a list - inverter stage IS.
The 2nd switch unit S2 can be additionally formed further in the 1st switch unit S1 list. The 2nd switch unit S2 is not important for the 1st switch unit S1 list to the function of the circuit apparatus of this invention.
: by which the component mentioned above is connected as follows mutually -- as for the 1st neurone metal oxide silicon field effect transistor M1, the output side AM 1 of the 1st neurone metal oxide silicon field effect transistor is connected to the output side ASP of SP of a current mirror through the 1st connection terminal 1. The output side AR of the criteria transistor R is connected to the input side ESP of SP of a current mirror. The input side EM 1 of the 1st neurone metal oxide silicon field effect transistor M1 and the output side ER of the criteria transistor R are connected to the 1st connection terminal A1S2 of the 2nd switch unit S2 through the 2nd connection terminal 2. The 2nd connection terminal A2S2 of the 2nd switch unit S2 is connected to ground potential. The 1st connection terminal 1 is connected to the 1st switch unit S1. The 1st switch unit S1 is further connected to the control connection terminal ST of the inverter stage IS.
Current mirror SP consists of two transistors M3 and M4. The inverter stage IS has two transistors M7 and M8. The 1st switch unit S1 has one transistor M6, and the 2nd switch unit S2 has one transistor M5. Current mirror SP's 1st connection terminal A2SP is connected to current mirror SP's 1st connection terminal A1SP list at action potential VDD. Similarly this action potential VDD is connected to the connection terminal BIS of the inverter stage IS. The connection terminal CIS of the inverter stage IS is grounded.
The control input side ES2 of the 2nd switch unit is connected to the control signal phi through the connection terminal 3 at the control input-side ES1 list of the 1st switch unit.
Floating-gate potential phiF of the 1st neurone metal oxide silicon field effect transistor is generated by the circuit apparatus of this invention explained above. This expresses the amount of inputs impressed to the gate connection terminal of the 1st neurone metal oxide silicon field effect transistor. The ratio of the 1st current I1 which flows the period of evaluation and the 1st neurone

metal oxide silicon field effect transistor M1, and the 1st current I2 which flows the criteria transistor R is the function of the difference of the floating-gate potential of the 1st neurone metal oxide silicon field effect transistor, and the floating-gate potential of the criteria transistor R. Active evaluation means that the circuit apparatus is activated by the 1st switch unit S1 list by the 2nd switch unit S2 in this relation. For this reason, there must be a control signal phi in an active state. When the control signal phi is switched high-level, the result of evaluation appears in the 1st connection terminal 1, and a still perfect CMOS stroke (CMOS-Hub) is not realized in that case. A perfect CMOS stroke is gradually realized in the output side AIS of the inverter stage IS.

The control signal phi after termination of evaluation is intercepted, and, thereby, the 1st switch unit S1 and the 2nd switch unit S2 are intercepted. Thereby, the decoupling from an original weighting network of the inverter stage IS and ground potential is performed. By taking out a charge at the gate of the transistors M7 and M8 of the inverter stage IS, Signal ES is held between time amount long enough in the output side AIS of the inverter stage IS as a result of the defined level, i.e., a comparison. The result signal ES can be succeedingly processed satisfactory in a consecutive circuit. It is realized that the level as which it has set to the output side AIS of the inverter stage IS, and does not define at the time of a gap with this circuit apparatus, either does not arise. It is directly switched to a new condition from an old condition. This property can be advantageously used in continuing data processing in a consecutive stage.

According to simulation, it turned out that the function of a circuit can evaluate certainly potential difference phiF in the floating gate of the 1st neurone metal oxide silicon field effect transistor M1 from 200mV. This has started that evaluation in the circuit apparatus of this invention is especially performed through the current which flows transistors M1 and M2, i.e., the current generated with the potential which joins low resistance at the gate of these transistors. Thereby, as for evaluation, strong and positive evaluation is realized to RF failure association.

Thereby, the narrow allowable deviation to a threshold type can also be maintained firmly.

The criteria transistor R can be formed in the 2nd one neurone metal oxide silicon field effect transistor M2 (refer to the 1st Fig.) list from one metal oxide silicon field effect transistor (refer to the 2nd Fig.). When the criteria transistor R consists of the 2nd neurone metal oxide silicon field effect transistor M2, at least two gate connection terminals are prepared, and the 1st gate connection terminal G1 is connected to action potential VDD in that case, and the 2nd gate connection terminal G2 is connected to the ground. In order to carry out an adjustment setup of the floating-gate potential of the 2nd neurone metal oxide silicon field effect transistor M2, therefore the change-over threshold of a weighting network at a precision, the 3rd gate connection terminal can be prepared.

When a metal oxide silicon field effect transistor is used as shown in Fig. 2, or it is supplied from the outside in this case, the reference voltage VRef generated inside is required. This is advantageous when asking for a precise adjustment setup of the gate potential of the criteria transistor R, therefore the change-over threshold of a weighting network. In case another advantage has only area with a metal oxide silicon field effect transistor slighter than a neurone metal oxide silicon field effect transistor and is used in a circuit, it is to be able to use the reference voltage which is changed into the 1st current I1 and which exists to the weighting network of the number of arbitration.

Use of the circuit apparatus of this invention for realizing a binary-multiplication machine cel is shown in Fig. 2. Binary-multiplication machine cel

は、２進乗算器セルの繰越ビットÜを形成するため

の第１の評価回路ＢÜと、２進乗算器セルの和ビッ

From the 2nd weighting network BS for forming TO s to ****

ている。第１の評価回路ＢÜも第２の評価回路ＢＳ

It ****s in the configuration of the circuit apparatus of ******** (refer to the 1st Fig.).

A binary-multiplication machine cel forms the product of two bits, and adds the partial product from another multiplier cel.
第１の評価回路ＢＵの第１のニューロンＭＯＳ電界

効果トランジスタＭＵ１のゲート接続端子も第２の評

The gate connection terminal of 1st neurone metal oxide silicon field effect transistor MS1 of ****** BS is also connected to the input potentials Va1, Va2, Vb, and Vc, respectively. In this case, in the input potential Va1, a multiplication child bit and the input potential Va2 express the multiplicand bit.
These bits are processed in a multiplier cel. The input potential Vb is the sum bit of the partial product to precede. The input potential Vc is the transfer bit of the partial product to precede. Input potentials Va1 and Va
２，V_bおよびV_cは第１の評価回路ＢＵの第１のニ

ューロンＭＯＳ電界効果トランジスタＭＵ１において

and 1st neurone metal oxide silicon field effect transistor MS1 of the 2nd weighting network BS -- setting -- Va1 and Va2 -- 1 time, and Vb and Vc -- this -- receiving -- relative -- twice -- ******** with weight -- like -- ******** with weight. **
１の評価回路ＢＵは第１の繰越ビットＵを形成する

。この繰越ビットＵは第２のインバータ段ＩＳ２を

It minds, and it is reversed and is added to another gate connection terminal of 1st neurone metal oxide silicon field effect transistor MS1 of the 2nd weighting network BS. Weighting of the denied transfer bit is 4 compared with weighting of the input potential Va1.
第１の評価回路ＢＵにおいて行われる、評価回路

ＢＵが活性化されている際の比較は、しきい値式の

技術的な実現である。第１の評価回路ＢＵの繰越ビッ

トＵの論理値は、制御信号Φが活性化されている場合

に第１の評価回路ＢＵの第１の電流I_{U1}が第１の評

価回路ＢＵの基準電流I_{U2}より大きいとき、そのと

きにだけ論理“１”である。第１の評価回路ＢＵの第

１のニューロンＭＯＳ電界効果トランジスタＭＵ１の

To weighting of above-mentioned input potential to a gate connection terminal
よって、第１の評価回路ＢＵは全体として次のしき

It is and a value expression is presented. : a1+a2+2b+2c> 3.5 (1)
a1 and a2 are the multiplication child bits and multiplicand bits which are processed in a multiplier cel here. The sum bit of the partial product to precede is expressed by Notation b. The transfer bit of the partial product to precede is expressed by Notation c.
The 2nd weighting network BS of a multiplier cel is close [which was explained above].

力電位と、上に説明した第１の評価回路ＢＵ̈の４倍

に重み付けられた否定された繰越ビットＵ̈から乗算

The sum bit s of a vessel cel is formed. In this case, it was denied.
繰越ビットＵ̈は値４によって重み付けられておりか

It connects with the gate connection terminal of 1st neurone metal oxide silicon field effect transistor MS1 of the weighting network BS of **** 2. The function of the 2nd weighting network BS ****s in a circuit apparatus of this invention mentioned above which was explained in Fig. 1. Therefore, the threshold expressed by the 2nd weighting network BS is as follows. :

$$a_1 + a_2 + 2_b + 2_b + 4\ \ddot{U} > 5.5 \qquad (2)$$

The variable in a top type expresses the same amount as the variable in a formula (1) here.
第２図の回路装置において、第１の評価回路ＢＵ̈

And the same reference signal is used to the 2nd weighting network BS. The condition of each threshold (3.5 thru/or 5.5) is acquired by adding the capacity to the active transistor field of the capacity to the floating gate of the input side of each neurone metal oxide silicon field effect transistor, and the floating gate, and doing a division by 2.
The following tables are shown in order to check the function of the binary-multiplication machine cel which the table of truth value to binary multiplication mentioned above. :

a_1	a_2	b	c	ü	s	$a_1/2+a_2/2+b+c$	$a_1/2+a_2/2+b+c-2ü$
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	0	1	0	0	1	1	1
0	0	1	1	1	0	2	0
0	1	0	0	0	0	0,5	0,5
0	1	0	1	0	1	1,5	1,5
0	1	1	0	0	1	1,5	1,5
0	1	1	1	1	0	2,5	0,5
1	0	0	0	0	0	0,5	0,5
1	0	0	1	0	1	1,5	1,5
1	0	1	0	0	1	1,5	1,5
1	0	1	1	1	0	2,5	0,5
1	1	0	0	0	1	1	1
1	1	0	1	1	0	2	0
1	1	1	0	1	0	2	0
1	1	1	1	1	1	3	1

Another example for constituting a binary-multiplication machine cel using the circuit apparatus of this invention is shown in Fig. 3.
ここで、基準トランジスタＲは第１の評価回路ＢＵ̈

To the neurone metal oxide silicon field effect transistor which can be boiled and set
って形成される。第１の評価回路ＢＵの構成はその

Others **** in Fig. 2. It differs from the 2nd weighting network BS shown in Fig. 2. However, in the 3rd weighting network BS 2 In the form where the transfer bit was denied, the gate connection terminal of 1st neurone metal oxide silicon field effect transistor MS12 of the 3rd weighting network BS 2 is not supplied. He is trying to supply another gate connection terminal of criteria neurone metal oxide silicon field effect transistor RS2 of the 3rd weighting network BS 2 directly in the form which is not denied. Therefore, the 3rd weighting network BS 2 shown in Fig. 3 will present the following inequality which ****s in the notation used until now. :

$$a_1 + a_2 + 2b + 2c < 1.5 + 4Ü \qquad (3)$$

Therefore, it compares for example, with a multiplicand bit, and a transfer bit is 4.
倍重み付けられている。全体の項（１．５＋４Ü）

Suitable selection of the input capacitance to the floating gate of ** and criteria neurone metal oxide silicon field effect transistor RS2 of the 3rd weighting network BS 2 realizes. it can set to the circuit apparatus of this invention at this selection and a list -- in addition to this, it exists -- altogether, the transistor is easily computable to this contractor, and he can carry it out.

[Translation done.]